

Design of a 32-b Monolithic Microprocessor Based on GaAs HMESFET Technology

Chien-Kuo V. Tien, Kelvin Lewis, Hans J. Gersch, Tom Tsien, and John F. McDonald

Abstract—This paper examines the design of a 32-b GaAs Fast RISC microprocessor (F-RISC/I). F-RISC/I is a single chip GaAs HMESFET processor targeted for implementation on a multichip module (MCM) together with cache memories. The CPU architecture, circuit design, implementation, and testing are optimized for a seven-stage instruction pipeline implemented with GaAs super-buffered FET logic (SBFL). We have been able to verify novel GaAs SBFL standard cells and compare measured CPU performance with performance estimates based on circuit and device models. The prototype 32-b microprocessor has been implemented using an automated standard cell approach because of time constraints and fabricated using an experimental process by Rockwell International. The CPU chip integrates 92 340 transistors on a $7 \times 7 \text{ mm}^2$ die and dissipates 6.13 W at 180 MHz. Test results from a prototype fabrication run have demonstrated the operation of the ALU, the program counter, and the register file with delays below 6, 5, and 3.4 ns, respectively. The successful modeling and verification indicate that a 0.5 μm HMESFET implementation of F-RISC/I could achieve a peak performance of 350 MHz. The wiring delays account for 42% of the critical path delay.

Index Terms—GaAs HMESFET, instruction pipeline, microprocessor design, multichip module (MCM), reduced instruction set computer (RISC), super-buffered FET logic (SBFL).

I. INTRODUCTION

Recent advances in GaAs Heterojunction MESFET (HMESFET) technology have led to gate delays below 100 ps [1] and higher integration levels, reaching VLSI complexity and, thereby, allowing the implementation of a 32-b GaAs RISC on a single chip [2]. However, integration levels are still very low compared to CMOS and do not allow the inclusion of sufficiently large caches on the chip. The cache memories must be implemented with high speed SRAM chips which need to be placed close to the CPU chip on an MCM to keep the interconnect delays low. The processor design, therefore, must consider the interactions between architecture, circuit technology, and MCM packaging. The main issues in GaAs microprocessor design are the processor versus memory speed mismatch and the limited off-chip communication bandwidth.

To overcome the difficulties of limited yield and low I/O bandwidth in GaAs, the high speed processing node, consisting of the processor and cache memory hierarchy, must be densely implemented on an MCM [3], [4]. F-RISC/I employs further a pipelined cache memory access [5] to "hide" some of the chip-to-chip delays in pipeline stages since, even on an MCM, the address and data transfer times between chips are of the same order as the processor delays.

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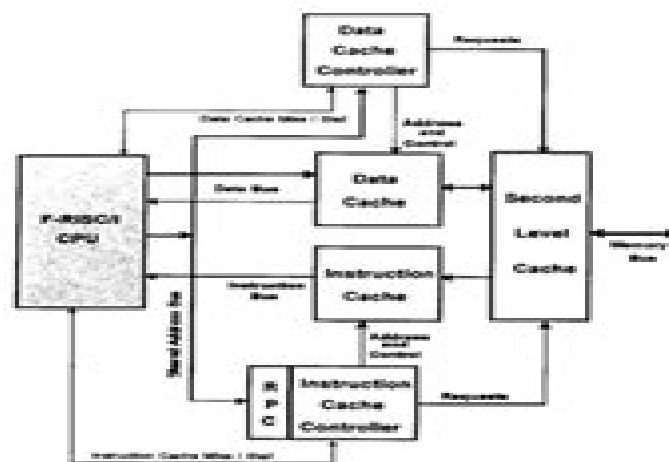


Fig. 1. F-RISC/I MCM system.

The primary goals of the Fast RISC/I (F-RISC/I) project were to verify the novel GaAs SBFL standard cells, to verify that HMESFET yields have reached adequate levels, and to correlate measured CPU performance with simulations based on circuit and device models to check the modeling capabilities of our CAD tools. F-RISC/I is a companion project to the ARPA sponsored heterojunction bipolar transistor (HBT) F-RISC project.

II. GAAS MICROPROCESSOR DESIGN

Fig. 1 shows the F-RISC/I MCM system. High memory bandwidth is achieved using separate instruction and data caches with their own data buses. This allows one 32-b instruction and one 32-b data word to be supplied by the cache memories in each cycle. A shared address bus is used to communicate with both the instruction and data cache memories to reduce CPU pin count and interconnections. This requires a remote program counter (RPC) on the instruction cache controller. Using the RPC the instruction cache can access consecutive instructions without an address transfer from the CPU. The instruction memory needs an address from the CPU only if a branch or an exception is taken. The shared address bus never causes contention in this scalar architecture since load/store and branch instructions are designed to use the address bus in the same pipeline stage.

The relative performance figure of a processor implementation is usually expressed in MIPS (millions of instructions per second), and is inversely proportional to the cycle time T_{cycle} and the average number of Cycles per Instruction (CPI). The principal parameters affecting T_{cycle} are the GaAs circuit technology and the pipeline. The CPI for a scalar RISC processor is basically one instruction cycle plus the average number of wasted cycles due to pipeline hazards, such as branch and load penalties, and stall cycles after cache misses. The CPU/system performance must be optimized by considering both the architecture (especially the pipeline scheme) and

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Microprocessor-design for GaAs Technology Veljko Milutinović, Purdue University. School of Electrical Engineering, 1986 **Microprocessor Design for GaAs Technology** Veljko Milutinović, 1990 **Foundations of Computer Technology** Alexander John Anderson, 2020-10-25 Foundations of Computer Technology is an easily accessible introduction to the architecture of computers and peripherals This textbook clearly and completely explains modern computer systems through an approach that integrates components systems software and design It provides a succinct systematic and readable guide to computers providing a springboard for students to pursue more detailed technology subjects This volume focuses on hardware elements within a computer system and the impact of software on its architecture It discusses practical aspects of computer organization structure behavior and design delivering the necessary fundamentals for electrical engineering and computer science students The book not only lists a wide range of terms but also explains the basic operations of components within a system aided by many detailed illustrations Material on modern technologies is combined with a historical perspective delivering a range of articles on hardware architecture and software programming methodologies and the nature of operating systems It also includes a unified treatment on the entire computing spectrum ranging from microcomputers to supercomputers Each section features learning objectives and chapter outlines Small glossary entries define technical terms and each chapter ends with an alphabetical list of key terms for reference and review Review questions also appear at the end of each chapter and project questions inspire readers to research beyond the text Short annotated bibliographies direct students to additional useful reading *Tutorial--gallium Arsenide Computer Design* Veljko Milutinović, David A. Fura, 1988 *Compound Semiconductor Electronics* Michael Shur, 1996 In many respects compound semiconductor technology has reached the age of maturity when applications will have been defined yields are high enough and well established and gallium arsenide and related compounds have carved many important niches in electronics This book reviews the state of the art of compound semiconductor electronics It covers the microwave millimeter wave and submillimeter wave devices monolithic microwave and digital integrated circuits made from compound semiconductors and emerging wide band semiconductor materials The book is written by leading experts in compound semiconductor electronics from industry and academia and strikes the balance between practical applications record breaking results and design and modeling tools specific for compound semiconductor technology Engineers scientists and graduate students working in solid state electronics and especially in the area of compound semiconductor electronics will find this book very useful It could also be used as a text or a supplementary text for graduate courses in this field

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