On Optimal Interconnections for VLSI
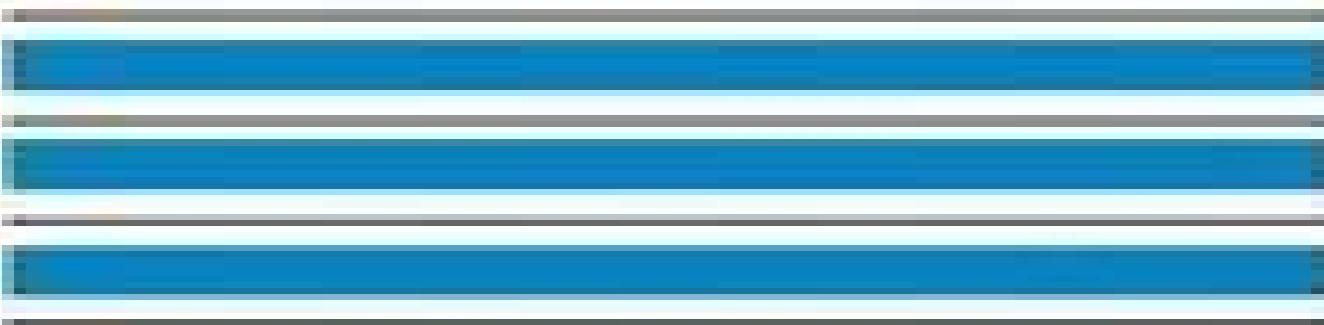
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On Optimal Interconnections for VLSI Andrew B. Kahng,Gabriel Robins,2013-04-17 On Optimal Interconnections for VLSI describes from a geometric perspective algorithms for high performance high density interconnections during the global and detailed routing phases of circuit layout First the book addresses area minimization with a focus on near optimal approximation algorithms for minimum cost Steiner routing In addition to practical implementations of recent methods the implications of recent results on spanning tree degree bounds and the method of Zelikovsky are discussed Second the book addresses delay minimization starting with a discussion of accurate yet algorithmically tractable delay models Recent minimum delay constructions are highlighted including provably good cost radius tradeoffs critical sink routing algorithms Elmore delay optimal routing graph Steiner arborescences non tree routing and wiresizing Third the book addresses skew minimization for clock routing and prescribed delay routing formulations The discussion starts with early matching based constructions and goes on to treat zero skew routing with provably minimum wirelength as well as planar clock routing Finally the book concludes with a discussion of multiple competing objectives i e how to optimize area delay skew and other objectives simultaneously These techniques are useful when the routing instance has heterogeneous resources or is highly congested as in FPGA routing multi chip packaging and very dense layouts Throughout the book the emphasis is on practical algorithms and a complete self contained development On Optimal Interconnections for VLSI will be of use to both circuit designers CAD tool users as well as researchers and developers in the area of performance driven physical design

Handbook of Algorithms for Physical Design Automation Charles J. Alpert,Dinesh P. Mehta,Sachin S. Sapatnekar,2008-11-12 The physical design flow of any project depends upon the size of the design the technology the number of designers the clock frequency and the time to do the design As technology advances and design styles change physical design flows are constantly reinvented as traditional phases are removed and new ones are added to accommodate changes in technology Handbook of Algorithms for Physical Design Automation provides a detailed overview of VLSI physical design automation emphasizing state of the art techniques trends and improvements that have emerged during the previous decade After a brief introduction to the modern physical design problem basic algorithmic techniques and partitioning the book discusses significant advances in floorplanning representations and describes recent formulations of the floorplanning problem The text also addresses issues of placement net layout and optimization routing multiple signal nets manufacturability physical synthesis special nets and designing for specialized technologies It includes a personal perspective from Ralph Otten as he looks back on the major technical milestones in the history of physical design automation Although several books on this topic are currently available most are either too broad or out of date Alternatively proceedings and journal articles are valuable resources for researchers in this area but the material is widely dispersed in the literature This handbook pulls together a broad variety of perspectives on the most challenging problems in the field and

focuses on emerging problems and research results   **Interconnect Analysis and Synthesis** Chung-Kuan Cheng,2000 State of the art methods and current perspectives on interconnect The irrepressible march toward smaller and faster integrated circuits has made interconnect a hot topic for semiconductor research The effects of wire size topology construction and network design on system performance and reliability have all been thoroughly investigated in recent years Interconnect Analysis and Synthesis provides CAD researchers and engineers with powerful state of the art tools for the analysis design and optimization of interconnect It brings together a wealth of information previously scattered throughout the literature explaining in depth available analysis techniques and presenting a range of CAD algorithms for synthesizing and optimizing interconnect Along with examples and results from the semiconductor industry and 150 illustrations this practical work features Models for interconnect as well as devices and the impact of scaling trends Modern analysis techniques from matrix reduction and moment matching to transmission line analysis An overview of the effects of inductance on on chip interconnect Flexible CAD algorithms that can be generalized for different needs from buffer insertion to wire sizing to routing topology Emphasis on realistic problem formulations addressing key design tradeoffs such as those between area and performance   **Microelectronic System Interconnections** Stuart K. Tewksbury,1994 Microelectronic system interconnections provides a uniques approach to the subject   Optimization of Copper Interconnection Circuits for 0.25um ULSI Technology Ka-Po Tsoi,1995   *VCSELs and Optical Interconnects* Hugo Thienpont,Jan Danckaert,2003   Circuit and System Performance Limits on ULSI Stanford University. Stanford Electronics Laboratories. Integrated Circuits Laboratory,Halil Burhan Bakoglu,1986   High Performance Integrated Circuit Design Emre Salman,Eby G. Friedman,2012-08-14 The latest techniques for designing robust high performance integrated circuits in nanoscale technologies Focusing on a new technological paradigm this practical guide describes the interconnect centric design methodologies that are now the major focus of nanoscale integrated circuits ICs High Performance Integrated Circuit Design begins by discussing the dominant role of on chip interconnects and provides an overview of technology scaling The book goes on to cover data signaling power management synchronization and substrate aware design Specific design constraints and methodologies unique to each type of interconnect are addressed This comprehensive volume also explains the design of specialized circuits such as tapered buffers and repeaters for data signaling voltage regulators for power management and phase locked loops for synchronization This is an invaluable resource for students researchers and engineers working in the area of high performance ICs Coverage includes Technology scaling Interconnect modeling and extraction Signal propagation and delay analysis Interconnect coupling noise Global signaling Power generation Power distribution networks CAD of power networks Techniques to reduce power supply noise Power dissipation Synchronization theory and tradeoffs Synchronous system characteristics On chip clock generation and distribution Substrate noise in mixed signal ICs Techniques to reduce substrate noise   **Proceedings of the ... International Conference on Microelectronics** ,2002

The Impact of Very High Performance Integrated Circuits on Radar, Guidance and Avionics Systems North Atlantic Treaty Organization. Advisory Group for Aerospace Research and Development. Avionics Panel. Symposium,1985

Parallel Architectures and Compilation Techniques Michel Cosnard,Guang R. Gao,Gabriel M. Silberman,1994 Fine and medium grain parallelism continues to hold its own as a vital vibrant research topic Within the area new developments in superscalar and VLIW architectures and their associated compilation techniques have provided exciting new avenues to extract performance from a slowing technology curve Comprising 28 full length papers and a number of short poster papers this publication offers a high quality exploration of the current state of the art in the field It will be of particular interest to those involved in control structures and microprogramming processor architectures computer system implementation programming techniques and software engineering **Quantum Well and Superlattice Physics** ,1987 *Index to IEEE Publications* Institute of Electrical and Electronics Engineers,1996 **Proceedings of the Workshop on Interconnection Networks for Parallel and Distributed Processing** ,1980 **Proceedings of the Workshop on Interconnection Networks for Parallel and Distributed Processing, April 21-22, 1980** Howard Jay Siegel,1980 **European Conference on Circuit Theory and Design, 5-8 September 1989** Institution of Electrical Engineers. Electronics Division,1989 **Proceedings** ,2007 **Conference Record** ,1988 1991 International Symposium on VLSI Technology, Systems and Applications ,1991 **Proceedings of ... International Conference on Information, Communications, and Signal Processing** ,1997

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