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# THE MIPS-X RISC MICROPROCESSOR

edited by

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# Mips X Risc Microprocessor

**Bank W. Lee, Bing J. Sheu**



## **Mips X Risc Microprocessor:**

**The MIPS-X RISC Microprocessor** Paul Chow, 2013-03-09 The first Stanford MIPS project started as a special graduate course in 1981 That project produced working silicon in 1983 and a prototype for running small programs in early 1984 After that we declared it a success and decided to move on to the next project MIPS X This book is the final and complete word on MIPS X The initial design of MIPS X was formulated in 1984 beginning in the Spring At that time we were unsure that RISC technology was going to have the industrial impact that we felt it should We also knew of a number of architectural and implementation flaws in the Stanford MIPS machine We believed that a new processor could achieve a performance level of over 10 times a VAX 11 780 and that a microprocessor of this performance level would convince academic skeptics of the value of the RISC approach We were concerned that the flaws in the original RISC design might overshadow the core ideas or that attempts to industrialize the technology would repeat the mistakes of the first generation designs MIPS X was targeted to eliminate the flaws in the first generation designs and to boost the performance level by over a factor of five *Library of Congress Subject Headings* Library of Congress, 2006 [A Practitioner's Guide to RISC Microprocessor Architecture](#) Patrick H. Stakem, 1996-04-25 Reduced Instruction Set Computers RISC reduce the number of instructions performed by the microprocessor This volume provides an overview of RISC as both a design philosophy and a marketing and technical force It introduces the fundamentals of RISC micro *Library of Congress Subject Headings* Library of Congress. Cataloging Policy and Support Office, 2000 *A Guide to RISC Microprocessors* Michael Slater, 1992 *Guide to RISC Processors* Sivarama P. Dandamudi, 2005-12-06 Details RISC design principles as well as explains the differences between this and other designs Helps readers acquire hands on assembly language programming experience *Compiler and Architecture Issues with CRegs* Peter J. Dahl, 1995 *Reduced Instruction Set Computers* William Stallings, 1990 **A Processor Architecture for Dynamic Memory Disambiguation** David Robert Engebretsen, 1997 **1991 International Symposium on VLSI Technology, Systems and Applications**, 1991 **A Guide to RISC Microprocessors** Florence Slater, 1992-06-03 A Guide to RISC Microprocessors provides a comprehensive coverage of every major RISC microprocessor family Independent reviewers with extensive technical backgrounds offer a critical perspective in exploring the strengths and weaknesses of all the different microprocessors on the market This book is organized into seven sections and comprised of 35 chapters The discussion begins with an overview of RISC architecture intended to help readers understand the technical details and the significance of the new chips along with instruction set design and design issues for next generation processors The chapters that follow focus on the SPARC architecture SPARC chips developed by Cypress Semiconductor in collaboration with Sun and Cypress's introduction of redesigned cache and memory management support chips for the SPARC processor Other chapters focus on Bipolar Integrated Technology's ECL SPARC implementation embedded SPARC processors by LSI Logic and Fujitsu the MIPS processor Motorola 88000 RISC chip set Intel 860 and 960 microprocessors

and AMD 29000 RISC microprocessor family This book is a valuable resource for consumers interested in RISC microprocessors    Field-programmable Logic and Applications ,1994    **A CRegs Implementation Study Based on the MIPS-X RISC Processor** Steve Nowakowski,Matthew T. O'Keefe,Army High Performance Computing Research Center,1991

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