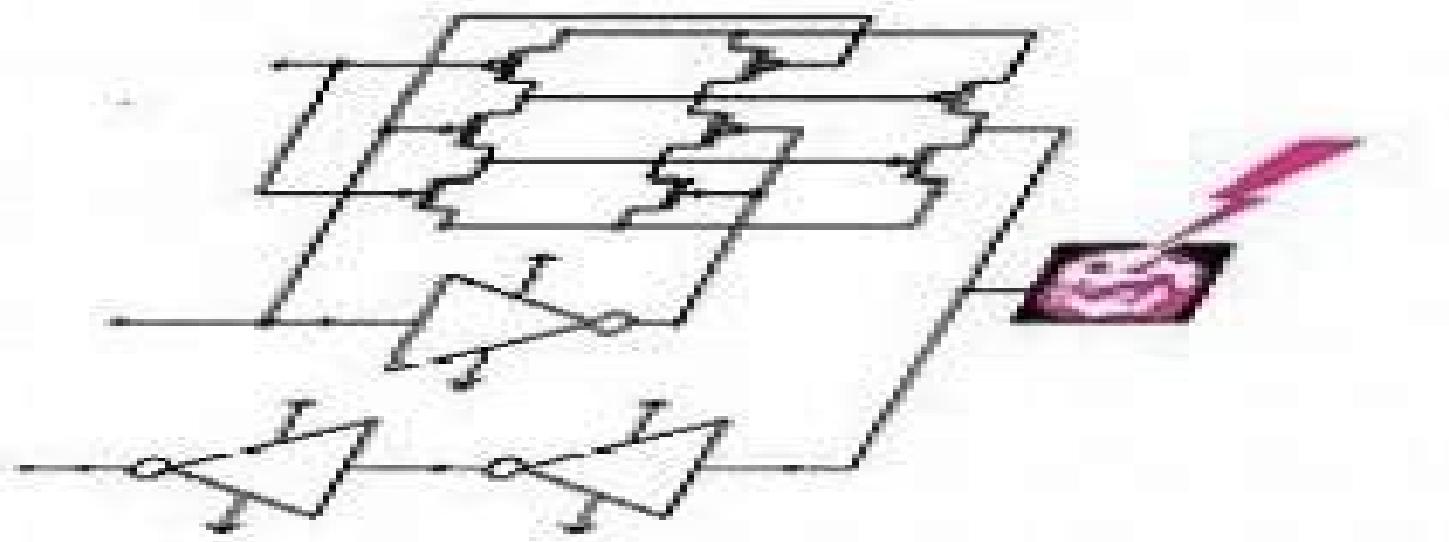


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# MODELING OF ELECTRICAL OVERSTRESS IN INTEGRATED CIRCUITS

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CARLOS H. DIAZ  
S.M. (STEVIE) KANG  
CHARVAKA DUVVURU

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# Modeling Of Electrical Overstress In Integrated Circuits

**E. Ajith Amerasekera,Charvaka  
Duvvury**

## **Modeling Of Electrical Overstress In Integrated Circuits:**

*Modeling of Electrical Overstress in Integrated Circuits* Carlos H. Diaz, Sung-Mo (Steve) Kang, Charvaka

Duvvury, 2012-12-06 Electrical overstress EOS and Electrostatic discharge ESD pose one of the most dominant threats to integrated circuits ICs. These reliability concerns are becoming more serious with the downward scaling of device feature sizes. Modeling of Electrical Overstress in Integrated Circuits presents a comprehensive analysis of EOS ESD related failures in I/O protection devices in integrated circuits. The design of I/O protection circuits has been done in a hit or miss way due to the lack of systematic analysis tools and concrete design guidelines. In general, the development of on chip protection structures is a lengthy expensive iterative process that involves tester design, fabrication, testing and redesign. When the technology is changed, the same process has to be repeated almost entirely. This can be attributed to the lack of efficient CAD tools capable of simulating the device behavior up to the onset of failure, which is a 3 D electrothermal problem. For these reasons, it is important to develop and use an adequate measure of the EOS robustness of integrated circuits in order to address the on chip EOS protection issue. Fundamental understanding of the physical phenomena leading to device failures under ESD/EOS events is needed for the development of device models and CAD tools that can efficiently describe the device behavior up to the onset of thermal failure. Modeling of Electrical Overstress in Integrated Circuits is for VLSI designers and reliability engineers, particularly those who are working on the development of EOS/ESD analysis tools. CAD engineers working on development of circuit level and device level electrothermal simulators will also benefit from the material covered. This book will also be of interest to researchers and first and second year graduate students working in semiconductor devices and IC reliability fields.

### **Modeling and Simulation of Electrical Overstress Failures in Input/output**

**Protection Devices of Integrated Circuits** Carlos Hernando Diaz, 1993 It is proposed in this thesis that a measure to determine the electrical overstress EOS hardness of integrated circuits with respect to ESD electrostatic discharge. ESD can be measured in terms of the power vs time to failure relationship power profile and the current vs time to failure relationship current profile. A new nonlinear mixed 2D/1D thermal simulator iTSIM was developed in order to understand and quantify the sensitivity of the power profiles with respect to major thermal parameters of the integrated circuit. IC Protection devices with different layout parameters were fabricated and experimentally characterized for EOS. Experimental data indicate that these devices fail with a poly gate filament in the drain edge when subjected to ESD or short duration EOS events while extensive device damage is observed for long duration EOS events revealing onset of thermal runaway. Two dimensional 2D device level electrothermal simulations are used to develop qualitative analysis of both the physical mechanisms leading to device failure and the dependencies of the failure thresholds power and current profiles on the layout parameters. Results from this study coupled with heat removal considerations led to a design guideline for source contact placement that is expected to improve the failure thresholds for I/O protection devices of CMOS ICs with grounded substrate. Thermal instability of an

electrically stressed circuit or device is shown to be the result of either thermally induced negative differential resistance NDR in resistive regions or junction second breakdown Under typical ESD EOS stress events transient in nature the temperature at which thermal instability takes place depends on the level of the stress current In semiconductor junctions reverse biased by an EOS event second breakdown is shown to happen at the time when thermal carrier generation becomes high enough to offset the effects of the mobility degradation and the reduction of the impact ionization rates Under these circumstances the time for the onset of second breakdown is shown to depend on the device s geometry and the level of power dissipation Circuit level electrothermal models are introduced for resistors diodes and bipolar and MOS transistors they are capable of describing device behaviour up into thermal runaway or second breakdown Abstract shortened by UMI

*On-Chip ESD Protection for Integrated Circuits* Albert Z.H. Wang,2006-01-03 This comprehensive and insightful book discusses ESD protection circuit design problems from an IC designer s perspective On Chip ESD Protection for Integrated Circuits An IC Design Perspective provides both fundamental and advanced materials needed by a circuit designer for designing ESD protection circuits including Testing models and standards adopted by U S Department of Defense EIA JEDEC ESD Association Automotive Electronics Council International Electrotechnical Commission etc ESD failure analysis protection devices and protection of sub circuits Whole chip ESD protection and ESD to circuit interactions Advanced low parasitic compact ESD protection structures for RF and mixed signal IC s Mixed mode ESD simulation design methodologies for design prediction ESD to circuit interactions and more Many real world ESD protection circuit design examples are provided The book can be used as a reference book for working IC designers and as a textbook for students in the IC design field

**Electrical Overstress/Electrostatic Discharge Symposium Proceedings** ,2004 **ESD Testing** Steven H. Voldman,2016-10-07 With the evolution of semiconductor technology and global diversification of the semiconductor business testing of semiconductor devices to systems for electrostatic discharge ESD and electrical overstress EOS has increased in importance ESD Testing From Components to Systems updates the reader in the new tests test models and techniques in the characterization of semiconductor components for ESD EOS and latchup Key features Provides understanding and knowledge of ESD models and specifications including human body model HBM machine model MM charged device model CDM charged board model CBM cable discharge events CDE human metal model HMM IEC 61000 4 2 and IEC 61000 4 5 Discusses new testing methodologies such as transmission line pulse TLP to very fast transmission line pulse VF TLP and future methods of long pulse TLP to ultra fast TLP UF TLP Describes both conventional testing and new testing techniques for both chip and system level evaluation Addresses EOS testing electromagnetic compatibility EMC scanning to current reconstruction methods Discusses latchup characterization and testing methodologies for evaluation of semiconductor technology to product testing ESD Testing From Components to Systems is part of the authors series of books on electrostatic discharge ESD protection this book will be an invaluable reference for the professional semiconductor chip

and system level ESD and EOS test engineer Semiconductor device and process development circuit designers quality reliability and failure analysis engineers will also find it an essential reference In addition its academic treatment will appeal to both senior and graduate students with interests in semiconductor process device physics semiconductor testing and experimental work

### **Transient-Induced Latchup in CMOS Integrated Circuits** Ming-Dou Ker,Sheng-Fu

Hsu,2009-07-23 The book all semiconductor device engineers must read to gain a practical feel for latchup induced failure to produce lower cost and higher density chips Transient Induced Latchup in CMOS Integrated Circuits equips the practicing engineer with all the tools needed to address this regularly occurring problem while becoming more proficient at IC layout Ker and Hsu introduce the phenomenon and basic physical mechanism of latchup explaining the critical issues that have resurfaced for CMOS technologies Once readers can gain an understanding of the standard practices for TLU Ker and Hsu discuss the physical mechanism of TLU under a system level ESD test while introducing an efficient component level TLU measurement setup The authors then present experimental methodologies to extract safe and area efficient compact layout rules for latchup prevention including layout rules for I O cells internal circuits and between I O and internal circuits The book concludes with an appendix giving a practical example of extracting layout rules and guidelines for latchup prevention in a 0 18 micrometer 1 8V 3 3V silicided CMOS process Presents real cases and solutions that occur in commercial CMOS IC chips Equips engineers with the skills to conserve chip layout area and decrease time to market Written by experts with real world experience in circuit design and failure analysis Distilled from numerous courses taught by the authors in IC design houses worldwide The only book to introduce TLU under system level ESD and EFT tests This book is essential for practicing engineers involved in IC design IC design management system and application design reliability and failure analysis

Undergraduate and postgraduate students specializing in CMOS circuit design and layout will find this book to be a valuable introduction to real world industry problems and a key reference during the course of their careers

### *ESD in Silicon Integrated Circuits* E. Ajith Amerasekera,Charvaka Duvvury,2002-05-22

Examines the various methods available for circuit protection including coverage of the newly developed ESD circuit protection schemes for VLSI circuits Provides guidance on the implementation of circuit protection measures Includes new sections on ESD design rules layout approaches package effects and circuit concepts Reviews the new Charged Device Model CDM test method and evaluates design requirements necessary for circuit protection

### **The ESD Handbook** Steven H. Voldman,2021-04-12

A practical and comprehensive reference that explores Electrostatic Discharge ESD in semiconductor components and electronic systems The ESD Handbook offers a comprehensive reference that explores topics relevant to ESD design in semiconductor components and explores ESD in various systems Electrostatic discharge is a common problem in the semiconductor environment and this reference fills a gap in the literature by discussing ESD protection Written by a noted expert on the topic the text offers a topic by topic reference that includes illustrative figures discussions and drawings The handbook covers a wide range of

topics including ESD in manufacturing garments wrist straps and shoes ESD Testing ESD device physics ESD semiconductor process effects ESD failure mechanisms ESD circuits in different technologies CMOS Bipolar etc ESD circuit types Pin Power Pin to Pin etc and much more In addition the text includes a glossary index tables illustrations and a variety of case studies Contains a well organized reference that provides a quick review on a range of ESD topics Fills the gap in the current literature by providing information from purely scientific and physical aspects to practical applications Offers information in clear and accessible terms Written by the accomplished author of the popular ESD book series Written for technicians operators engineers circuit designers and failure analysis engineers The ESD Handbook contains an accessible reference to ESD design and ESD systems *Basic ESD and I/O Design* Sanjay Dabral,Timothy Maloney,1998 This volume presents an integrated treatment of ESD I/O and process parameter interactions that both I/O designers and process designers can use It examines key factors in I/O and ESD design and testing and helps the reader consider ESD and reliability issues up front when making I/O choices Emphasizing clarity and simplicity this book focuses on design principles that can be applied widely as this dynamic field continues to evolve

**Electrical Overstress (EOS)** Steven H. Voldman,2013-08-27 Electrical

Overstress EOS continues to impact semiconductor manufacturing semiconductor components and systems as technologies scale from micro to nano electronics This book teaches the fundamentals of electrical overstress and how to minimize and mitigate EOS failures The text provides a clear picture of EOS phenomena EOS origins EOS sources EOS physics EOS failure mechanisms and EOS on chip and system design It provides an illuminating insight into the sources of EOS in manufacturing integration of on chip and system level EOS protection networks followed by examples in specific technologies circuits and chips The book is unique in covering the EOS manufacturing issues from on chip design and electronic design automation to factory level EOS program management in today's modern world Look inside for extensive coverage on Fundamentals of electrical overstress from EOS physics EOS time scales safe operating area SOA to physical models for EOS phenomena EOS sources in today's semiconductor manufacturing environment and EOS program management handling and EOS auditing processing to avoid EOS failures EOS failures in both semiconductor devices circuits and system Discussion of how to distinguish between EOS events and electrostatic discharge ESD events e.g. such as human body model HBM charged device model CDM cable discharge events CDM charged board events CBE to system level IEC 61000-4-2 test events EOS protection on chip design practices and how they differ from ESD protection networks and solutions Discussion of EOS system level concerns in printed circuit boards PCB and manufacturing equipment Examples of EOS issues in state of the art digital analog and power technologies including CMOS LDMOS and BCD EOS design rule checking DRC LVS and ERC electronic design automation EDA and how it is distinct from ESD EDA systems EOS testing and qualification techniques and Practical off chip ESD protection and system level solutions to provide more robust systems Electrical Overstress EOS Devices Circuits and Systems is a continuation of the author's series of books on ESD protection It is an essential reference

and a useful insight into the issues that confront modern technology as we enter the nano electronic era **Istfa '98** ASM International,1998-01-01 **Electrostatic Discharge Protection** Juin J. Liou,2017-12-19 Electrostatic discharge ESD is one of the most prevalent threats to electronic components In an ESD event a finite amount of charge is transferred from one object i e human body to another i e microchip This process can result in a very high current passing through the microchip within a very short period of time Thus more than 35 percent of single event chip damages can be attributed to ESD events and designing ESD structures to protect integrated circuits against the ESD stresses is a high priority in the semiconductor industry Electrostatic Discharge Protection Advances and Applications delivers timely coverage of component and system level ESD protection for semiconductor devices and integrated circuits Bringing together contributions from internationally respected researchers and engineers with expertise in ESD design optimization modeling simulation and characterization this book bridges the gap between theory and practice to offer valuable insight into the state of the art of ESD protection Amply illustrated with tables figures and case studies the text Instills a deeper understanding of ESD events and ESD protection design principles Examines vital processes including Si CMOS Si BCD Si SOI and GaN technologies Addresses important aspects pertinent to the modeling and simulation of ESD protection solutions Electrostatic Discharge Protection Advances and Applications provides a single source for cutting edge information vital to the research and development of effective robust ESD protection solutions for semiconductor devices and integrated circuits *Proceedings of the ... Custom Integrated Circuits Conference* ,1986 *1993 IEEE International Symposium on Circuits and Systems* ,1993 Texas Instruments Technical Journal ,1994 **International Aerospace Abstracts** ,1999 *American Book Publishing Record* ,1995 *Electronic Materials Handbook* ,1989-11-01 Volume 1 Packaging is an authoritative reference source of practical information for the design or process engineer who must make informed day to day decisions about the materials and processes of microelectronic packaging Its 117 articles offer the collective knowledge wisdom and judgement of 407 microelectronics packaging experts authors co authors and reviewers representing 192 companies universities laboratories and other organizations This is the inaugural volume of ASMs all new ElectronicMaterials Handbook series designed to be the Metals Handbook of electronics technology In over 65 years of publishing the Metals Handbook ASM has developed a unique editorial method of compiling large technical reference books ASMs access to leading materials technology experts enables to organize these books on an industry consensus basis Behind every article Is an author who is a top expert in its specific subject area This multi author approach ensures the best most timely information throughout Individually selected panels of 5 and 6 peers review each article for technical accuracy generic point of view and completeness Volumes in the Electronic Materials Handbook series are multidisciplinary to reflect industry practice applied in integrating multiple technology disciplines necessary to any program in advanced electronics Volume 1 Packaging focusing on the middle level of the electronics technology size spectrum offers the greatest practical value to the largest and broadest group of users Future

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