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Lsi Vsli Testability Design

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LSI/VLSI Testability Design Frank F. Tsui, 1987 **LSI/VLSI Design for Testability Analysis and General Approach**, 1982 **Design for Testability in LSI/VLSI Systems** F. F. Tsui, 1986 **State-of-the-Art Assessment of Testing and Testability of Custom LSI/VLSI Circuits. Volume V. Design for Testability** A. J. Carlan, AEROSPACE CORP EL SEGUNDO CA ENGINEERING GROUP., 1982

Designing for testability if needed to reduce costs associated with testing and maintaining electronic systems Two approaches are considered 1 modification of established circuits and 2 general design of new circuits where testability is a major consideration Computer programs TMEAS and SCOAP developed for evaluating testability in established circuits are discussed In the design of new circuits only a few techniques are known that yield highly testable circuits without sacrificing other desirable traits two IBM s LSSD method and bit slicing are discussed Author

Scientific and Technical Aerospace Reports, 1984-04 **LSI (Large Scale Integrated) Design for Testability. Final Report of Design, Demonstration, and Testability Analysis** R. D. Groves, R. L. Schoenike, IBM FEDERAL SYSTEMS DIV MANASSAS VA., 1983

The objective of this effort was to demonstrate IBM Level Sensitive Scan Design methodology as an approach for improving the testability of military LSI VLSI circuits LSSD was demonstrated in an LSI component AP101C test bed to be a viable and attractive design approach for military LSI VLSI components Author Digital VLSI Systems Mohamed I. Elmasry, 1985 *VLSI Fault Modeling and Testing Techniques* George W. Zobrist, 1993

VLSI systems are becoming very complex and difficult to test Traditional stuck at fault problems may be inadequate to model possible manufacturing defects in the integrated circuit Hierarchical models are needed that are easy to use at the transistor and functional levels Stuck open faults present severe testing problems in CMOS circuits to overcome testing problems testable designs are utilized Bridging faults are important due to the shrinking geometry of ICs BIST PLA schemes have common features controllability and observability which are enhanced through additional logic and test points Certain circuit topologies are more easily testable than others The amount of reconvergent fan out is a critical factor in determining realistic measures for determining test generation difficulty Test implementation is usually left until after the VLSI data path has been synthesized into a structural description This leads to investigation methodologies for performing design synthesis with test incorporation These topics and more are discussed Tutorial Test Generation for VLSI Chips Vishwani D. Agrawal, 1988

The ... International Conference on Computers and Applications, 1987 *State-of-the-Art Assessment of Testing and Testability of Custom LSI/VLSI Circuits. Volume II. Hardware Design Verification* A. J. Carlan, AEROSPACE CORP EL SEGUNDO CA., 1982

The complexity of digital circuits requires that more emphasis be placed on design specifications and verification Specification of design requirements currently advocated is done with formal hardware descriptive languages HDLs to describe hardware function Industry s current use of HDLs is primarily for simulation Verifying a design is a less mature discipline Three approaches are considered simulation symbolic simulation and formal proofs While symbolic

simulation shows promise much research and development is required *The Second International Conference on Computers and Applications, Beijing (Peking), People's Republic of China, June 23-27, 1987 ,1987* Computer Aided Design, Modelling and Simulation International Association of Science and Technology for Development,1986

State-of-the-Art Assessment of Testing and Testability of Custom LSI/VLSI Circuits. Volume I. Executive Summary M. A. Breuer, Al J. Carlan, AEROSPACE CORP EL SEGUNDO CA ENGINEERING GROUP.,1982 This project is a two phase study dealing with testing and testability of custom LSI VLSI circuits The tasks summarized and evaluated in this report consisted of compiling and documenting a survey and assessment of the state of the art for each of seven topics Each of these topics has resulted in a formal report and are listed below Vol 2 Hardware Design Verification Vol 3 Fault Mode Analysis Vol 4 Test Generation Vol 5 Design for Testability Vol 6 Redundancy Testing Circuits and Codes Vol 7 Built in Testing BIT and Built in Test Equipment BITE and Vol 8 Fault Simulation **Selected Reprints on Logic Design for Testability** Constantin C.

Timoc,1984 *The Future of Test* ,1985 **Fault Tolerant and Fault Testable Hardware Design** Parag K. Lala,1985

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