

# MATCHING PROPERTIES OF DEEP SUB-MICRON MOS TRANSISTORS

Jeroen A. Croon, Willy Sansen  
and Herman E. Maes



# Matching Properties Of Deep Sub Micron Mos Transistors

**Gennady Gildenblat**

## **Matching Properties Of Deep Sub Micron Mos Transistors:**

**Matching Properties of Deep Sub-Micron MOS Transistors** Jeroen A. Croon, Willy M. Sansen, Herman E. Maes, 2006-06-20 Matching Properties of Deep Sub Micron MOS Transistors examines this interesting phenomenon. Microscopic fluctuations cause stochastic parameter fluctuations that affect the accuracy of the MOSFET. For analog circuits this determines the trade off between speed power accuracy and yield. Furthermore due to the down scaling of device dimensions transistor mismatch has an increasing impact on digital circuits. The matching properties of MOSFETs are studied at several levels of abstraction. A simple and physics based model is presented that accurately describes the mismatch in the drain current. The model is illustrated by dimensioning the unit current cell of a current steering D/A converter. The most commonly used methods to extract the matching properties of a technology are bench marked with respect to model accuracy measurement accuracy and speed and physical contents of the extracted parameters. The physical origins of microscopic fluctuations and how they affect MOSFET operation are investigated. This leads to a refinement of the generally applied 1 area law. In addition the analysis of simple transistor models highlights the physical mechanisms that dominate the fluctuations in the drain current and transconductance. The impact of process parameters on the matching properties is discussed. The impact of gate line edge roughness is investigated which is considered to be one of the roadblocks to the further down scaling of the MOS transistor. Matching Properties of Deep Sub Micron MOS Transistors is aimed at device physicists, characterization engineers, technology designers, circuit designers or anybody else interested in the stochastic properties of the MOSFET.

**Matching Properties of Deep Sub-Micron MOS Transistors** Jeroen A. Croon, Willy M. C. Sansen, Herman E. Maes, 2008-11-01 Matching Properties of Deep Sub Micron MOS Transistors examines this interesting phenomenon. Microscopic fluctuations cause stochastic parameter fluctuations that affect the accuracy of the MOSFET. For analog circuits this determines the trade off between speed power accuracy and yield. Furthermore due to the down scaling of device dimensions transistor mismatch has an increasing impact on digital circuits. The matching properties of MOSFETs are studied at several levels of abstraction. A simple and physics based model is presented that accurately describes the mismatch in the drain current. The model is illustrated by dimensioning the unit current cell of a current steering D/A converter. The most commonly used methods to extract the matching properties of a technology are bench marked with respect to model accuracy measurement accuracy and speed and physical contents of the extracted parameters. The physical origins of microscopic fluctuations and how they affect MOSFET operation are investigated. This leads to a refinement of the generally applied 1 area law. In addition the analysis of simple transistor models highlights the physical mechanisms that dominate the fluctuations in the drain current and transconductance. The impact of process parameters on the matching properties is discussed. The impact of gate line edge roughness is investigated which is considered to be one of the roadblocks to the further down scaling of the MOS transistor. Matching Properties of Deep Sub Micron MOS Transistors

is aimed at device physicists characterization engineers technology designers circuit designers or anybody else interested in the stochastic properties of the MOSFET     **Stochastic Process Variation in Deep-Submicron CMOS** Amir

Zjajo,2013-11-19 One of the most notable features of nanometer scale CMOS technology is the increasing magnitude of variability of the key device parameters affecting performance of integrated circuits The growth of variability can be attributed to multiple factors including the difficulty of manufacturing control the emergence of new systematic variation generating mechanisms and most importantly the increase in atomic scale randomness where device operation must be described as a stochastic process In addition to wide sense stationary stochastic device variability and temperature variation existence of non stationary stochastic electrical noise associated with fundamental processes in integrated circuit devices represents an elementary limit on the performance of electronic circuits In an attempt to address these issues Stochastic Process Variation in Deep Submicron CMOS Circuits and Algorithms offers unique combination of mathematical treatment of random process variation electrical noise and temperature and necessary circuit realizations for on chip monitoring and performance calibration The associated problems are addressed at various abstraction levels i e circuit level architecture level and system level It therefore provides a broad view on the various solutions that have to be used and their possible combination in very effective complementary techniques for both analog mixed signal and digital circuits The feasibility of the described algorithms and built in circuitry has been verified by measurements from the silicon prototypes fabricated in standard 90 nm and 65 nm CMOS technology     **Tradeoffs and Optimization in Analog CMOS Design** David

Binkley,2008-09-15 Analog CMOS integrated circuits are in widespread use for communications entertainment multimedia biomedical and many other applications that interface with the physical world Although analog CMOS design is greatly complicated by the design choices of drain current channel width and channel length present for every MOS device in a circuit these design choices afford significant opportunities for optimizing circuit performance This book addresses tradeoffs and optimization of device and circuit performance for selections of the drain current inversion coefficient and channel length where channel width is implicitly considered The inversion coefficient is used as a technology independent measure of MOS inversion that permits design freely in weak moderate and strong inversion This book details the significant performance tradeoffs available in analog CMOS design and guides the designer towards optimum design by describing An interpretation of MOS modeling for the analog designer motivated by the EKV MOS model using tabulated hand expressions and figures that give performance and tradeoffs for the design choices of drain current inversion coefficient and channel length performance includes effective gate source bias and drain source saturation voltages transconductance efficiency transconductance distortion normalized drain source conductance capacitances gain and bandwidth measures thermal and flicker noise mismatch and gate and drain leakage current Measured data that validates the inclusion of important small geometry effects like velocity saturation vertical field mobility reduction drain induced barrier lowering and inversion level

increases in gate referred flicker noise voltage In depth treatment of moderate inversion which offers low bias compliance voltages high transconductance efficiency and good immunity to velocity saturation effects for circuits designed in modern low voltage processes Fabricated design examples that include operational transconductance amplifiers optimized for various tradeoffs in DC and AC performance and micropower low noise preamplifiers optimized for minimum thermal and flicker noise A design spreadsheet available at the book web site that facilitates rapid optimum design of MOS devices and circuits Tradeoffs and Optimization in Analog CMOS Design is the first book dedicated to this important topic It will help practicing analog circuit designers and advanced students of electrical engineering build design intuition rapidly optimize circuit performance during initial design and minimize trial and error circuit simulations

### **Compact Modeling**

Gennady Gildenblat,2010-06-22 Most of the recent texts on compact modeling are limited to a particular class of semiconductor devices and do not provide comprehensive coverage of the field Having a single comprehensive reference for the compact models of most commonly used semiconductor devices both active and passive represents a significant advantage for the reader Indeed several kinds of semiconductor devices are routinely encountered in a single IC design or in a single modeling support group Compact Modeling includes mostly the material that after several years of IC design applications has been found both theoretically sound and practically significant Assigning the individual chapters to the groups responsible for the definitive work on the subject assures the highest possible degree of expertise on each of the covered models

Microelectronic Device Technology ,1999      *Charge-Based MOS Transistor Modeling* Christian C. Enz, Eric A. Vittoz,2006-08-21 Modern large scale analog integrated circuits ICs are essentially composed of metal oxide semiconductor MOS transistors and their interconnections As technology scales down to deep sub micron dimensions and supply voltage decreases to reduce power consumption these complex analog circuits are even more dependent on the exact behavior of each transistor High performance analog circuit design requires a very detailed model of the transistor describing accurately its static and dynamic behaviors its noise and matching limitations and its temperature variations The charge based EKV Enz Krummenacher Vittoz MOS transistor model for IC design has been developed to provide a clear understanding of the device properties without the use of complicated equations All the static dynamic noise non quasi static models are completely described in terms of the inversion charge at the source and at the drain taking advantage of the symmetry of the device Thanks to its hierarchical structure the model offers several coherent description levels from basic hand calculation equations to complete computer simulation model It is also compact with a minimum number of process dependant device parameters Written by its developers this book provides a comprehensive treatment of the EKV charge based model of the MOS transistor for the design and simulation of low power analog and RF ICs Clearly split into three parts the authors systematically examine the basic long channel intrinsic charge based model including all the fundamental aspects of the EKV MOST model such as the basic large signal static model the noise model and a discussion of temperature effects and

matching properties the extended charge based model presenting important information for understanding the operation of deep submicron devices the high frequency model setting out a complete MOS transistor model required for designing RF CMOS integrated circuits Practising engineers and circuit designers in the semiconductor device and electronics systems industry will find this book a valuable guide to the modelling of MOS transistors for integrated circuits It is also a useful reference for advanced students in electrical and computer engineering

### **Charge-Based MOS Transistor Modeling**

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Linearization of CDMA Receiver Front-ends Vladimir Aparin, 2005 **Proceedings IECON. ,1999 IECON '99 IEEE Industrial Electronics Society. Conference, IEEE Industrial Electronics Society, 1999** This text constitutes proceedings from the Annual Conference of the Industrial Electronics Society IECON which took place in 1999 Topics covered include control and signal processing for microlithography process autonomous mobile robots and fuzzy logic

### **Nano-CMOS Circuit and Physical Design**

Ban Wong, 2005 Based on the authors expansive collection of notes taken over the years Nano CMOS Circuit and Physical Design bridges the gap between physical and circuit design and fabrication processing manufacturability

and yield This innovative book covers process technology including sub wavelength optical lithography impact of process scaling on circuit and physical implementation and low power with leaky transistors and DFM yield and the impact of physical implementation *Chemical Abstracts* ,2002 **ICMTS 2002** ,2002 **Power Conscious and Robust Design Methods for the SUB-90NM CMOS Digital Circuit** Harmander Singh Deogun,2006 **Proceedings of the Fifth Workshop on Electronics for LHC Experiments** University of Wisconsin-Madison,1999 *Annales des télécommunications* ,2002 *Digital Calibration for Low-power High-performance A/D Conversion* Boris Murmann,2003 *Proceedings* ,2004 *13th Symposium on Integrated Circuits and Systems Design* Ricardo Augusto da Luz Reis,Jose Carlos Monteiro,Wilhelmus Van Noije,2000 These papers are taken from 13th Brazilian Symposium on Integrated Circuit Design SBCCI 2000 They address issues such as microarchitectures architecture logic design analogue design high level synthesis digital design physical modelling reconfigurable hardware and more

## Unveiling the Power of Verbal Artistry: An Psychological Sojourn through **Matching Properties Of Deep Sub Micron Mos Transistors**

In a world inundated with monitors and the cacophony of fast interaction, the profound power and mental resonance of verbal artistry usually diminish into obscurity, eclipsed by the regular assault of noise and distractions. Yet, set within the musical pages of **Matching Properties Of Deep Sub Micron Mos Transistors**, a charming perform of literary brilliance that impulses with natural emotions, lies an memorable trip waiting to be embarked upon. Composed by way of a virtuoso wordsmith, this interesting opus guides readers on a psychological odyssey, softly revealing the latent possible and profound affect stuck within the complex web of language. Within the heart-wrenching expanse of the evocative examination, we shall embark upon an introspective exploration of the book is central subjects, dissect its charming publishing fashion, and immerse ourselves in the indelible effect it leaves upon the depths of readers souls.

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