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Multilevel Interconnect Technology

Gopal K. Rao

Multilevel Interconnection Technology

Ih-Chin Chen

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Multilevel Interconnect Technology ,1998   Low Temperature Multilevel Interconnection Technology Employing a Polyimide James William Peterson,1985   Multilevel Interconnect Technology Gopal K. Rao,1993 The first book on a key topic in IC technology Table of Contents Multilevel Interconnection Design Multilevel Interconnect Processing Manufacturing Reliability Index 100 illustrations   Microelectronic Device and Multilevel Interconnection Technology ,1996   Copper Interconnect Technology Christoph Steinbruchel,Barry Chin,2001 A textbook designed to accompany The Society of Photo Optical Instrumentation Engineers short course on improving interconnect performance for increased speed in overall circuit performance authored by Steinbrnchel materials science and engineering Renselaer Polytechnic Institute and Chin senio

Advanced Interconnects for ULSI Technology Mikhail Baklanov,Paul S. Ho,Ehrenfried Zschech,2012-02-17 Finding new materials for copper low k interconnects is critical to the continuing development of computer chips While copper low k interconnects have served well allowing for the creation of Ultra Large Scale Integration ULSI devices which combine over a billion transistors onto a single chip the increased resistance and RC delay at the smaller scale has become a significant factor affecting chip performance Advanced Interconnects for ULSI Technology is dedicated to the materials and methods which might be suitable replacements It covers a broad range of topics from physical principles to design fabrication characterization and application of new materials for nano interconnects and discusses Interconnect functions characterisations electrical properties and wiring requirements Low k materials fundamentals advances and mechanical properties Conductive layers and barriers Integration and reliability including mechanical reliability electromigration and electrical breakdown New approaches including 3D optical wireless interchip and carbon based interconnects Intended for postgraduate students and researchers in academia and industry this book provides a critical overview of the enabling technology at the heart of the future development of computer chips   **A Multilevel Planar Interconnect Technology Utilizing the Selective Deposition of Tungsten** David Charles Thomas,1990   Handbook of Semiconductor Manufacturing Technology Yoshio Nishi,Robert Doering,2000-08-09 The Handbook of Semiconductor Manufacturing Technology describes the individual processes and manufacturing control support and infrastructure technologies of silicon based integrated circuit manufacturing many of which are also applicable for building devices on other semiconductor substrates Discussing ion implantation rapid thermal processing photomask fabrication chip testing and plasma etching the editors explore current and anticipated equipment devices materials and practices of silicon based manufacturing The book includes a foreword by Jack S Kilby cowinner of the Nobel Prize in Physics 2000 for his part in the invention of the integrated circuit   Copper Interconnect Technology Tapan Gupta,2010-01-22 Since overall circuit performance has depended primarily on transistor properties previous efforts to enhance circuit and system speed were focused on transistors as well During the last decade however the parasitic resistance capacitance and inductance associated with interconnections began

to influence circuit performance and will be the primary factors in the evolution of nanoscale ULSI technology Because metallic conductivity and resistance to electromigration of bulk copper Cu are better than aluminum use of copper and low k materials is now prevalent in the international microelectronics industry As the feature size of the Cu lines forming interconnects is scaled resistivity of the lines increases At the same time electromigration and stress induced voids due to increased current density become significant reliability issues Although copper low k technology has become fairly mature there is no single book available on the promise and challenges of these next generation technologies In this book a leader in the field describes advanced laser systems with lower radiation wavelengths photolithography materials and mathematical modeling approaches to address the challenges of Cu interconnect technology *Interconnect Technology and Design for Gigascale Integration* Jeffrey A. Davis,James D. Meindl,2012-12-06 Interconnect Technology and Design for Gigascale Integration is the cumulative effort from academic researchers at Georgia Tech MIT and Stanford as well as from industry researchers at IBM T J Watson Research Center LSI Logic and SUN microsystems The material found in this book is unique in that it spans IC interconnect topics ranging from IBM s revolutionary copper process to an in depth exploration into interconnect aware computer architectures This broad swath of topics presented by leaders in the research field is intended to provide a comprehensive perspective on interconnect technology and design issues so that the reader will understand the implications of the semiconductor industry s next substantial milestone gigascale integration **Proceedings** ,1990 **Interconnect and Contact Metallization for ULSI** G. S. Mathad,Hamir Singh Rathore,Y. Arita,2000 **Proceedings .... International IEEE VLSI Multilevel Interconnection Conference** ,1989 **Multilevel Interconnection** Hoang H. Hoang,1993 Eighth International IEEE VLSI Multilevel Interconnection Conference, 1991 IEEE Electron Devices Society,1991 **Handbook of Multilevel Metallization for Integrated Circuits** Syd R. Wilson,Clarence J. Tracy,John L. Freeman,1993 It is widely recognized that the successful design development and integration of multilevel metallization MLM systems is and will continue to be key to current and future VLSI technologies All major semiconductor companies have significant ongoing research teams focused in this area These teams must view multilevel metallization as a system rather than a collection of isolated process modules Microelectronic Device and Multilevel Interconnection Technology Ih-Chin Chen,Society of Photo-optical Instrumentation Engineers,1995 **Microelectronic Device and Multilevel Interconnection Technology II** Ih-Chin Chen,1996-01-01 **ULSI Technology** C. Y. Chang,S. M. Sze,1996 This text follows the tradition of Sze s highly successful pioneering text on VLSI technology and is updated with the latest advances in the field of microelectronic chip fabrication Since computer chips are foundations of modern electronics these topics are essential for the next generation of USLI technologies allowing more transistors to be packaged on a single chip Contributing to each chapter are industry experts specializing in topics such as epitaxy with low temperature process rapid thermal processes low damage plasma reactive ion etching fine line litography cleaning technology clean room technology packing

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