
THE MIPS-X RISC MICROPROCESSOR

edited by

Paul Chow

University of Toronto



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The MIPS-X RISC Microprocessor Paul Chow, 2013-03-09 The first Stanford MIPS project started as a special graduate course in 1981 That project produced working silicon in 1983 and a prototype for running small programs in early 1984 After that we declared it a success and decided to move on to the next project MIPS X This book is the final and complete word on MIPS X The initial design of MIPS X was formulated in 1984 beginning in the Spring At that time we were unsure that RISC technology was going to have the industrial impact that we felt it should We also knew of a number of architectural and implementation flaws in the Stanford MIPS machine We believed that a new processor could achieve a performance level of over 10 times a VAX 11 780 and that a microprocessor of this performance level would convince academic skeptics of the value of the RISC approach We were concerned that the flaws in the original RISC design might overshadow the core ideas or that attempts to industrialize the technology would repeat the mistakes of the first generation designs MIPS X was targeted to eliminate the flaws in the first generation designs and to boost the performance level by over a factor of five

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set Intel 860 and 960 microprocessors and AMD 29000 RISC microprocessor family This book is a valuable resource for consumers interested in RISC microprocessors **Field-programmable Logic and Applications** ,1994 *A CRegs Implementation Study Based on the MIPS-X RISC Processor* Steve Nowakowski,Matthew T. O'Keefe,Army High Performance Computing Research Center,1991 *Design, Implementation and Use of the MIRV Experimental Compiler for Computer Architecture Research* David Anthony Greene,2003 RISC Architectures J.C. Heudin,C. Panetto,1992-05-31 This book covers the principles and techniques that make RISC a unique and elegant approach for high performance microprocessor system designs describing both the practical and theoretical aspects of the RISC design philosophy **Hardware Annealing in Analog VLSI Neurocomputing** Bank W. Lee,Bing J. Sheu,1990-12-31 Rapid advances in neural sciences and VLSI design technologies have provided an excellent means to boost the computational capability and efficiency of data and signal processing tasks by several orders of magnitude With massively parallel processing capabilities artificial neural networks can be used to solve many engineering and scientific problems Due to the optimized data communication structure for artificial intelligence applications a neurocomputer is considered as the most promising sixth generation computing machine Typical applications of artificial neural networks include associative memory pattern classification early vision processing speech recognition image data compression and intelligent robot control VLSI neural circuits play an important role in exploring and exploiting the rich properties of artificial neural networks by using programmable synapses and gain adjustable neurons Basic building blocks of the analog VLSI neural networks consist of operational amplifiers as electronic neurons and synthesized resistors as electronic synapses The synapse weight information can be stored in the dynamically refreshed capacitors for medium term storage or in the floating gate of an EEPROM cell for long term storage The feedback path in the amplifier can continuously change the output neuron operation from the unity gain configuration to a high gain configuration The adjustability of the voltage gain in the output neurons allows the implementation of hardware annealing in analog VLSI neural chips to find optimal solutions very efficiently Both supervised learning and unsupervised learning can be implemented by using the programmable neural chips **The Cumulative Book Index** ,1992 A world list of books in the English language **Proceedings of Technical Papers** ,1991 **The Indispensable Pentium Book** Hans-Peter Messmer,1995 Providing a unique comparison with competing RISC implementations The Indispensable Pentium Book offers a comprehensive treatment of this important processor for all PC programmers *1995 IEEE TENCON* Institute of Electrical and Electronics Engineers. Region 10. Conference on Microelectronics and VLSI,1995

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