



Network Processor Design

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Network Processor Design Issues And Practices

Terry C. Jones



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Network Processor Design Mark A. Franklin, Patrick Crowley, Haldun Hadimioglu, Peter Z. Onufryk, 2005-03-11 The past few years have seen significant change in the landscape of high end network processing In response to the formidable challenges facing this emerging field the editors of this series set out to survey the latest research and practices in the design programming and use of network processors Through chapters on hardware software performance and modeling Network Processor Design illustrates the potential for new NP applications helping to lay a theoretical foundation for the architecture evaluation and programming of networking processors Like Volume 2 of the series Volume 3 further shifts the focus from achieving higher levels of packet processing performance to addressing other critical factors such as ease of programming application developments power and performance prediction In addition Volume 3 emphasizes forward looking leading edge research in the areas of architecture tools and techniques and applications such as high speed intrusion detection and prevention system design and the implementation of new interconnect standards Investigates current applications of network processor technology at Intel Infineon Technologies and NetModule Presents current research in network processor design in three distinct areas Architecture at Washington University St Louis Oregon Health and Science University University of Georgia and North Carolina State University Tools and Techniques at University of Texas Austin Academy of Sciences China University of Paderborn Germany and University of Massachusetts Amherst Applications at University of California Berkeley Universidad Complutense de Madrid Spain ETH Zurich Switzerland Georgia Institute of Technology Vrije Universiteit the Netherlands and Universiteit Leiden the Netherlands

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Technologies Intel Corp North Carolina State University Swiss Federal Institute of Technology University of California Berkeley University of Dortmund University of Washington and Washington University Examines the latest network processors from Agere Systems Cisco IBM Intel Motorola Sierra Inc and TranSwitch **Network Processor Design** Mark A. Franklin, Patrick Crowley, Haldun Hadimioglu, Peter Z. Onufryk, 2002-10-16 As the demand for digital communication networks has increased so have the challenges in network component design To meet ever escalating performance flexibility and economy requirements the networking industry has opted to build products around network processors These new chips range from task specific processors such as classification and encryption engines to more general purpose packet or communications processors Programmable yet application specific their designs are tailored to efficiently implement communications applications such as routing protocol analysis voice and data convergence firewalls VPNs and QoS Network processor design is an emerging field with issues and opportunities both numerous and formidable To help meet this challenge the editors of this volume created the first Workshop on Network Processors a forum for scientists and engineers from academia and industry to discuss their latest research in the architecture design programming and use of these devices In addition to including the results of the Workshop in this volume the editors also present specially commissioned material from practicing designers who discuss their companies latest network processors Network Processor Design Issues and Practices is an essential reference on network processors for graduate students researchers and practicing designers Includes contributions from major academic and industrial research labs including Aachen University of Technology Cisco Systems Infineon Technologies Intel Corp North Carolina State University Swiss Federal Institute of Technology University of California Berkeley University of Dortmund University of Washington and Washington University Examines the latest network processors from Agere Systems Cisco IBM Intel Motorola Sierra Inc and TranSwitch **Network Processor Design**, 2004 **Network Processor Design - Issues And Practices** Patrick Crowley, 2004-01-01 **Network Processor Design**, 2004 **High Performance Switches and Routers** H. Jonathan Chao, Bin Liu, 2007-05-23 As Internet traffic grows and demands for quality of service become stringent researchers and engineers can turn to this go to guide for tested and proven solutions This text presents the latest developments in high performance switches and routers coupled with step by step design guidance and more than 550 figures and examples to enable readers to grasp all the theories and algorithms used for design and implementation **Network Processors** Panos C. Lekkas, 2003-07-28 Table of contents **Applications of Multi-objective Evolutionary Algorithms** Carlos A. Coello Coello, Gary B. Lamont, 2004 Detailed MOEA applications discussed by international experts State of the art practical insights in tackling statistical optimization with MOEAs A unique monograph covering a wide spectrum of real world applications Step by step discussion of MOEA applications in a variety of domains Building ASIPs: The Mescal Methodology Matthias Gries, Kurt Keutzer, 2005-06-28 An increasing number of system designers are using ASIP s rather than ASIC s to implement their system solutions Building

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The IEEE Computer Society's 12th Annual International Symposium on Modeling, Analysis, and Simulation of Computer and Telecommunications Systems (MASCOTS 2004), 2004 MASCOTS 2004 looks at how models can be calibrated and validated against real world observations The papers explore wireless and mobile networks networks and protocols stochastic models queueing networks Internet architecture and applications P2P systems routing algorithms and storage systems

Processor Efficiency for Packet-processing Applications Elizabeth Seamans, 2005

IEEE International Workshop on Workload Characterization, 2003

Programming Models for Application-specific Instruction Processors Niraj Rajnikant Shah, 2004

Application Specific Embedded Processor Customizations for Low Power and High Performance Peter Petrov, 2004

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CASES 2003 Jaime H. Moreno, Praveen K. Murthy, 2003

Proceedings of the 36th Annual IEEE/ACM International Symposium on Microarchitecture, 2003 MICRO 36 discusses new microarchitecture and software techniques and explores the latest research related to processor architecture compilers and systems for technical interaction on traditional MICRO topics The proceedings also places a special emphasis on optimizations that take advantage of application specific opportunities In addition this year s MICRO includes papers that will benefit both the microarchitecture and embedded architecture communities

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